DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION

ABSTRACT OF THE DISCLOSURE

Accordingly, the present invention provides a double gated transistor and a method for forming the same that results in improved device performance and density. The preferred embodiment of the present invention uses provides a double gated transistor with asymmetric gate doping, where one of the double gates is doped degenerately n-type and the other degenerately p-type. By doping on of the gates n-type, and the other p-type, the threshold voltage of the resulting device is improved. In particular, by asymmetrically doping the two gates, the resulting transistor can, with adequate doping of the body, have a threshold voltage in a range that enables low-voltage CMOS operation. For example, a transistor can be created that has a threshold voltage between 0V and 0.5V for nFETs and between 0 and -0.5V for pFETs.